Výstupy (deliverables) projektu:				
por.č.	**názov výstupu:**	**typ/druh výstupu:**	**stručný popis výstupu:**	**obdobie (v mesiacoch) od začiatku realizácie projektu potrebné pre dosiahnutie výstupu:**
1.	**Proof of massive parallel chip integration of ADC-based wireless receivers with >200MHz bandwidth in cheap 28-20nm technology**	Chip design completed: MPW 2. Prototype to be fabricated in 28-20nm technology	Technical locks: Broadband counteracts low power ADC, thus novel ADC architecture needs to be evaluated, multichanel integration challange Technical challenge to solve the technical locks: Expertise in broadband Sigma-Delta systems and design of multi-path broadband amplifiers, novel DAC in SigmaDelta Feedback, adaptive calibration	29
2.	**Proof of massive-parallel single-chip integration of multi-channel ADC wireless MIMO SDR receiver**	Multichanel chip design completed: MPW 2. Prototype to be fabricated in 180-130nm technology	Technical challenge to solve the technical locks: Investigation of ultralow-power (µW) design techniques on lowest possible chip area for interfacing neuromorphic systems. Chip prototype ready to co-nitegrate neuromorphic devices from Bizzcom.	29