výstupy (deliverables) projektu:				
por.č.	**názov výstupu:**	**typ/druh výstupu:**	**stručný popis výstupu:**	**obdobie (v mesiacoch) od začiatku realizácie projektu potrebné pre dosiahnutie výstupu:**
1.	**functional device stack for the filamentary memristor**	**Prototype**	Different electrode materials (TiN, Ta, Ni, Pt) will be researched and the PE-ALD fabrication process will be tuned to obtain feasible characteristics ● fast <100 ns switching, evaluated by pulsed measurements using Keithley 4200 SCS ● high device-to-device uniformity of the switching voltages Vmin/Vmax ● high cycling endurance ● identification of the tuning knobs for achieving required values of Vmin/Vmax	12
2.	**functional device stack for the analogue memristor**	**Prototype**	A bi-layer oxide will be deposited using PE-ALD, exploiting preferably Al2O3/HfO2 and HfO2/TiO2 structures. PE-ALD process tuning will be employed in order to engineer the stoichiometry profile in these bi-layered oxides to achieve satisfactory analogue memristive behaviour with a focus on the following characteristics ● evaluation of the effect of thickness and stoichiometry of the first oxide layer (switching oxide) on the resistance window, operation voltage and breakdown voltage ● evaluation of the effect of the thickness of the second oxide layer (barrier oxide) on the operation current level ● area-dependence of the operation current ● state retention ● cycling endurance / resistance drift ● temperature effects ● dynamic behaviour - memristor response (resistance change) to different voltage pulses	12

3.	**implementation into the crossbar array configuration, establishing ideal array sizes, line resistance effects**	**Prototype**	The fabrication of the memristor arrays will require different lithography masks as compared to single devices but the deposition processes will be equal to the single device. Following characteristics will be studied using the probe card and a switching relay: ● array yield ● effect of electrode line thickness on the line resistance ● effect of array size on the line resistance and subsequent device-to-device switching uniformity ● effect of operation current on the sneak path currents	24
4.	**fine-tuning based on the understanding of trade-offs which govern the relationships between different memristor characteristics**	**Analysis**	Number of memristors in the crossbar will be tested by repetitive switching and readout cycles and their electrical parameters will be monitored. Namely, we will focus on the measurement of ON- and OFF-state resistance for given switching voltage and their ratio as a function of number of cycles (up to 106). Possible parasitic drift of these parameters will be evaluated and parametrized. Further, time dependence of the electrical parameters will be examined in stress/recovery experiments and possible reversible and irreversible changes will be identified. Temperature dependence of reversible and irreversible changes will be then evaluated and characterized, depending on the observed temperature dependence.	30
5.	**System design**	**Digital prototype**	Analog Circuit Design of ADC/DAC blocks, Physical Mask Design, Digital HDL Design	30
6.	**Fuzzy logic function HW design (for analog, digital and ADC/DAC parts)**	**Digital prototype**	SPICE-simulation and verification of ADC and DAC analog and digital block connectivity	30